## Fowler-Nordheim Erasing Time Prediction in Flash Memory

Pierre Canet<sup>1</sup>, Valéry Bouquet<sup>1,2</sup>, Frédéric Lalande<sup>1</sup>, Jean Devin<sup>2</sup>, Bruno Leconte<sup>2</sup>
(1) L2MP-UMR CNRS 6137, IMT Technopole de Château Gombert, 13451 Marseille Cedex 13
(2) ST-Microelectronics, ZI de Rousset BP 2, 13106 Rousset Cedex, FRANCE

## **Abstract**

Programming of a Flash memory cell used two different mechanisms: a fast Channel Hot Electrons Injection in programming mode (with programming time of about  $\mu$ s) and a slow Fowler Nordheim injection in erasing mode (with erasing time of about ms).

In order to pre-evaluate the necessary time needed to write a flash cell memory (programming or erasing), we use a simplified expression for the Fowler Nordheim injecting current during the erase mode which is the longer one.

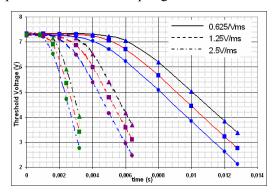
This allows us to find a relationship between the applied voltages and the resulting threshold voltage.

$$I_{FN} = g \times (V_S - V_{FG})$$

We show in this study that the absolute value of the derivative of the threshold voltage is equal to the positive signal slope applied on the control gate.

$$\frac{dV_T}{dt} = -\frac{dV_{GC}}{dt}$$

We validate this assumption by measurements on samples provided by ST-Microelectronics with different slope and with samples with different coupling ratios.



**Figure** Threshold voltage evolution in erase mode for three memory cells with different coupling ratios ( $\triangle$  cell A,  $\alpha_G$ =0.61;  $\blacksquare$  cell B,  $\alpha_G$ =0.71;  $\bullet$  cell C,  $\alpha_G$ =0.78) by three positive signal slopes (0.625V/ms; 1.25V/ms; 2.5V/ms).

In order to reduce this erasing time, we need a better modelling of the Fowler Nordheim injecting current, especially during the establishment of the current.

## References

- [1] W.D. Brown, J.E. Brewer, Non Volatile Semi-conductor Memory Technology, IEEE Press (1998).
- [2] R. H Fowler and L. Nordheim, Proc. Soc. London Ser., A119 (1928) 173.
- [3] B. Eitan, D. Froham-Bentchkowsky, Hot-Electron Injection into the Oxyde in N-Channel MOS devices, IEEE Trans. Electron Devices, ED-28 n°3 (1981) 328-340.
- [4] C. Hu, Lucky Electron Model for Channel Hot-Electron Emission, IEDM Tech. Dig., (1979) 22.
- [5] P. Canet, R. Bouchakour, F. Lalande, J.M. Mirabel, EEPROM Cell Design: Paradoxical Choice of the Coupling Ratio, J. Non-Cryst. Solids, vol. 322 (2003) p.246-249.
- [6] V. Bouquet, P. Canet, F. Lalande, R. Bouchakour, J.M. Mirabel, Non Volatile Memory Cell Design: Coupling Ratio Impact On tunnel Oxide Reliability, J. Non-Cryst. Solids (2005) to be published.
- [7] P. Canet, F. Lalande, J. Razafindramora, V. Bouquet, J. Postel, R. Bouchakour, J.M. Mirabel, Integrated Reliability in Non Volatile Memory Cell Design, NVMTS'2004 5th Annual Non-Volatile Memory Technology Symposium, Orlando, Florida, November 15-17 (2004) proceeding CD.